REMARKS

Favorable reconsideration of the application is respectfully requested in light of the amendments and remarks herein.

Upon entry of this amendment, claims 1, 3, and 5–12 will be pending. By this amendment, claims 1 and 9 have been amended. No new matter has been added.

§103 Rejection of Claims 1, 3 and 7–12

In Sections 5–12 of the Final Office Action, claims 1, 3 and 7–12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sobel *et al.* (U.S. Patent No. 6,707,937; hereinafter referred to as "Sobel") in view of Okada (U.S. Patent No. 6,133,953).

In the Background of the Specification it was disclosed that "[o]ptical imaging equipment such as cameras ... are typically provided with an imaging lens, which focuses light to form an image." *Specification, page 1, lines 19–20.* "However, lenses to not form a perfect representation of the image ... because optical properties of the lens itself cause distortion in the focused image ... such [as] chromatic aberration." *Specification, page 2, lines 6–9.* "It is known ... to improve the quality of an image represented by a video signal by compensating for the effects of the chromatic aberration ... by interpolating between parts of the image within a field of the video signal." *Specification, page 2, lines 14–19.* "[I]t remains a technical problem to improve the compensating effects of interpolation to images affected *inter alia* by chromatic error. *Specification, page 3, lines 12–14.*

To solve the problem described above, embodiments of the present invention provide for an "adaptable shift register [having] a plurality of register elements, selected register elements

being connected to [an] interpolator to provide the pixels of the received video signal for interpolation, each of the register elements being arranged to store a pixel of the received video signal and each may be connected to a plurality of other register elements and may be configurable under control of [a] control processor to feed the pixel element stored in the register element to one or other of the other shift registers in accordance with a temporal reference." *Specification, page 4, lines 11–17.* (emphasis added) "[P]ixels may be shifted through the adaptable register store to the effect of providing the co-sited pixels of a particular part of the image to be interpolated. Interpolation is therefore effected on the contents of the selected register elements. [B]y controlling which subsequent register element a pixel value held in a current register element is to be communicated, a two dimensional set of spatially related pixels is available, without requiring a frame store. This is particularly advantageous because frame stores are expensive." *Specification, page 4, lines 20–26.*

For example, claim 1, as recited herein, provides for:

> *An image processor* arranged in operation to generate an interpolated video signal from a received video signal representative of an image, said image processor comprising:
>
> *a register store* comprising a *plurality of register elements* and being coupled to a *control processor*,
>
> said register store being arranged in operation to receive said video signal and to provide pixels of said received video signal, under control of said control processor to an *interpolator*,
>
> *selected register elements* being connected to said interpolator to provide said pixels of said received video signal for interpolation,
>
> each of said plurality of register elements being arranged to store a pixel of said received video signal, two or more of said plurality of register elements having

> an input connected to a first plurality of other register elements and
>
> an output connected to a second plurality of other register elements,
>
> and each of said two or more of said plurality of register elements is
>
> > configurable under control of said control processor to feed the pixel stored in said register element to one of said plurality of other register elements to which said register element is connected in accordance with a temporal reference,
>
> said interpolator being coupled to said register store and arranged in operation to generate said interpolated video signal by interpolating said pixels provided by said register store,
>
> wherein said control processor is operable to detect a feature of said image having both vertical and horizontal components, to control the configuration of said register elements to provide the input pixels associated with said feature to said interpolator to interpolate the feature of said image having both the vertical and the horizontal components.
>
> (emphasis added)

Accordingly, in one aspect of claim 1, the image processor is characterized such that a register store comprises a plurality of register elements where two or more of said plurality of register elements have an input connected to a first plurality of other register elements and an output connected to a second plurality of other register elements.

Moreover, "[a]s can be seen in FIG. 10 each register element is connected to more than one register element in the subsequent column. The register elements are at least connected to the register element in the corresponding row in the next column. Furthermore the register elements are connected to the register element in the row above and the row below in the next

column except where the register element is in the first and last rows. In this case then the register elements are only connected to the row below and the row above in the subsequent column respectively." *Specification, page 16, lines 13–19.*

By contrast, Sobel fails to teach or suggest a register store comprising a plurality of register elements where two or more of said plurality of register elements have an input connected to a first plurality of other register elements and an output connected to a second plurality of other register elements.

Further, Okada was cited for disclosing a 2-D register array connected to an interpolation processing circuit. However, the two dimensional register array disclosed by Okada merely includes serially connected registers which output a 1 clock delayed signal. *Okada, Fig. 3 and Col. 7, lines 21–25.* Thus, Okada also fails to teach or suggest a register store comprising a plurality of register elements where two or more of said plurality of register elements have an input connected to a first plurality of other register elements and an output connected to a second plurality of other register elements. It is therefore maintained that Sobel and Okada, individually or in combination, fail to teach or suggest all the limitations of claim 1.

Based on the foregoing discussion, claim 1 should be allowable over Sobel and Okada. Since claim 9, as amended herein, parallels and recites substantially similar limitations as recited in claim 1, claim 9 should also be allowable over Sobel and Okada. Further, since claims 3, 7–8 and 10–12 depend from one of claims 1 and 9, claims 3, 7–8 and 10–12 should also be allowable over Sobel and Okada.

Accordingly, it is submitted that the rejection of claims 1, 3 and 7–12 based upon 35 U.S.C. §103(a) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

Allowable Subject Matter

In Section 13 of the Office Action, claims 5 and 6 stand objected to as being dependent on a rejected base claim. It is appreciatively noted that claims 5 and 6 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

As discussed above, however, it is submitted that the rejection of independent claim 1 has been overcome. Since claims 5 and 6 depend from claim 1, it is maintained that claims 5 and 6 are also allowable. Therefore, it is respectfully requested that the objection to claims 5 and 6 be withdrawn.

Conclusion

In view of the foregoing, entry of this amendment, and the allowance of this application with claims 1, 3 and 5–12 are respectfully solicited.

In regard to the claims amended herein and throughout the prosecution of this application, it is submitted that these claims, as originally presented, are patentably distinct over the prior art of record, and that these claims were in full compliance with the requirements of 35 U.S.C. §112. Changes that have been made to these claims were not made for the purpose of patentability within the meaning of 35 U.S.C. §§101, 102, 103 or 112. Rather, these changes were made simply for clarification and to round out the scope of protection to which Applicant is entitled.

In the event that additional cooperation in this case may be helpful to complete its prosecution, the Examiner is cordially invited to contact Applicant's representative at the telephone number written below.

The Commissioner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account 50-0320.

Respectfully submitted,

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